



VLIW instruction slot assign

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**A fill-unit approach to multiple instruction issue - group of 4 »**

M Franklin, M Smotherman - 27th Intl. Symp. on Microarchitecture, 1994 - portal.acm.org

... The **VLIW instruction** format exactly represents the functionality and number of resources on a given im- ... together in one **VLIW instruction**. ...

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**Instruction Scheduling for Clustered VLIW Architectures - group of 13 »**

FJ Sanchez, A Gonzalez - ISSS, 2000 - doi.ieeecomputersociety.org

... **VLIW Instruction** ... employs a unified **assign-and-schedule** approach, as proposed by Özer et al. ... possible cluster (ie those clusters with an empty **slot** for the ...

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**Flexible Issue Slot Assignment for VLIW Architectures - group of 4 »**

Z Chamski, C Eisenbeis, E Rohou - RAPPORT DE RECHERCHE-INSTITUT NATIONAL DE RECHERCHE EN ... , 1999 - inria.fr

... the TriMedia, each **VLIW instruction** contains several slots. In each of these slots, only some specified types of operations can take place. For instance, in **slot 1** ...

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**Compiler optimization on VLIW instruction scheduling for low power - group of 5 »**

C Lee, JK Lee, T Hwang, SC Tsai - ACM Transactions on Design Automation of Electronic Systems, 2003 - portal.acm.org

... i and j if microinstruction i can be scheduled into the same position, or **slot**, in the whole **VLIW instruction** as the position of microinstruction u ...

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**Inter-Cluster Communication Models for Clustered VLIW Processors - group of 10 »**

A Terechko, EL Thenaff, M Garg, JTH Eindhoven, H ... - HPCA, 2003 - ieeexplore.ieee.org

... lead to expansion of the **VLIW instruction**, complicating the **instruction** decoder.

Moreover, this ICC model needs two extra RF ports per dedicated **slot** and the ...

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**Modulo scheduling for a fully-distributed clustered VLIW architecture - group of 10 »**

J Sanchez, A Gonzalez - MICRO-ANNUAL WORKSHOP THEN ANNUAL INTERNATIONAL SYMPOSIUM-, 2000 - portal.acm.org

... In the example, the **VLIW instruction** that contains the ... the number of cycles that the **instruction** stalls is ... the clusters in which there is an available **slot**. ...

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**Automatic generation of application specific processors - group of 3 »**

D Goodwin, D Petkov - Proc. of Int'l Conf. on Compilers, Architecture, and ... , 2003 - portal.acm.org

... **Instruction** Formats x24: size 24 bits, 1 **slot slot** Inst: size 24 ... Figure 3: Example configuration generated for SAD example for **VLIW** issue width of 1 and ...

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**Automatic Design of VLIW and EPIC Instruction Formats - group of 5 »**

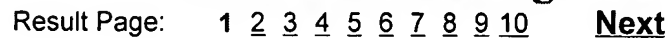
S Aditya, BR Rau, R Johnson - HP LABORATORIES TECHNICAL REPORT HPL, 2000 - fog.hpl.external.hp.com

... execution in a **VLIW** or EPIC processor ... We define the canonical **instruction** format

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